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09/501,493	02/09/2000	John Marland Garth	ST9-99-130	3937

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EXAMINER	
VO, LILIAN	

ART UNIT	PAPER NUMBER
2127	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/501,493	Applicant(s) GARTH ET AL.	
	Examiner Lilian Vo	Art Unit 2127	

-- The MAILING DATE of this communication app ars on the cover sh et with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 57* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 11, 20 - 30 and 39 - 49* is/are rejected.

7)☒ Claim(s) *12 - 19, 31 - 38 and 50 - 57* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-57 are pending.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 20, and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bayer et al. (US Pat 5,202,987, hereinafter Bayer) in view of Tsuchida et al. (US Pat 6,026,394, hereinafter Tsuchida).

4. Regarding **claims 1, 20, and 39**, Bayer teaches a method of loading data into a data store connected to a computer, the method comprising the steps of:

identifying memory constraints (col. 1, lines 13 – 15, memory and processors are operations bottleneck and col. 5, lines 52 – 56, memory is constrained or limited through factors such as physical shared storage, network access or processor distribution, and common memory space);

identifying processing capabilities (col. 1, lines 17 – 27, synchronization activities are controlled by algorithm, which depends on processing power and col. 5, lines 24 – 31 requires the number of processors and capabilities of each processor, which entail processing capabilities); and

determining a number of load (col. 14, lines 25 – 33, loading capacity being part of task map) to be started in parallel based on the identified memory constraints and processing capabilities (col. 7, lines 9 – 1).

Although Bayer teaches the sort process being a mere tasks allocation to the processors (col. 1, lines 44 – 50), Tsuchida has nevertheless further detailed the sort feature, which includes the step of determining a number of sort processes (col. 8, lines 50 – 51 disclose the fact that the sorting process depends on the number of node for join process. Col. 7, lines 54 – 57 show that the number of join nodes for performing merge process can be determined. Hence, number of sort processes is a known quantity).

It is considered obvious to one of ordinary skill in the art, at the time the invention was made, to combine the sorting feature shown by Tsuchida to the invention of Bayer so that sort processing time, which is a factor in load balancing processes can be determined as part of system characteristics and optimization purposes (Tsuchida: col. 7, line 58 – col. 8, line 35). Note that the sort steps shown by Tsuchida are also parallel processes as claimed in the application (fig. 3, parallel pipeline operation).

5. Claims 1, 20, and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bhattacharya et al. (US Pat 5,797,000, hereinafter Bhattacharya).

6. As per **claims 1, 20, and 39**, Bhattachary teaches a method of loading data into a data store connected to a computer, the method comprising the steps of:

identifying memory constraints (col. 9, lines 6 – 7, memory becomes a constraint as its capacity is a contributing factor and is limited);

identifying processing capabilities (fig. 1, number of processors p, col. 4, line 41 – col. 5, line 8, each processor is assigned with a specific number of tasks, hence indicating each limited capability); and

determining a number of load (col. 3, lines 1 – 3, join column domain and tuples are the load, which obviously much be known in order for them to be partitioned and transferred among the cluster, col. 3, lines 7 - 18), and sort processes (col. 2, line 62 – col. 3, line 6 disclose various method of parallel sort process in which merge join is one example. Since the actual tasks assigned to the processors are determined during the join phase, which is part of the sort process as shown above, number of sort processes are hence inherently determined as well) to be started in parallel based on the identified memory constraints and processing capabilities (col. 1, lines 24

– 28, col. 4, line 64 – col. 5, line 8: parallel tasks based on processing capabilities, col. 2, lines 66 – col. 3, line 6: parallel sort processing).

7. Claims 2 – 3, 21 – 22, and 40 - 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bhattacharya et al. (US Pat 5,797,000, hereinafter Bhattacharya) as applied to claims 1, 20, and 39 above, in view of Hintz et al. (US Pat 5,222,235, hereinafter Hintz).

8. Regarding **claim 2**, although Bhattacharya did not teach the step determining a number of build processes based on the number of sort processes, nevertheless, this teaching is considered common knowledge in the art per Hintz's invention (col. 5, lines 50 – 51).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to realize this common feature shown by Hintz to the invention of Bhattacharya as one in the pertained art would know that build process is a consequential step directly dependent on sort process.

9. Regarding **claim 3**, Bhattacharya fails to teach the number of sort processes does not exceed a number of indexes to be built. Nevertheless, according to Hintz's teachings (col. 5, lines 50 - 51), "one index at a time" clearly indicates the claimed invention, in which the number of indexes excessive to the number of sort processes would not be possible.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to integrate this feature as taught by Hintz to the invention of Bhattacharya so that the number of build indexes can not exceed the number of sort processes.

10. **Claims 21 – 22 and 40 – 41** are rejected on the same ground as stated above.

11. Claims 4 – 6, 23 – 25, and 42 - 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bhattacharya et al. (US Pat 5,797,000, hereinafter Bhattacharya) as applied to claims 1, 20, and 39 above, in view of Bordonaro et al. (US Pat 5,307,485, hereinafter Bordonaro).

12. Regarding **claim 4,** Bhattacharya fails to teach the number of load processes does not exceed a number of partitions to be loaded. Nevertheless, this feature has been taught by Bordonaro (fig. 3, 310 shows N partitioned tasks and 312 distributes over the N processors). In fig. 2, 202 shows that as the records from storage device are loaded, col. 4, line 62 – col. 6, line 27 describes the fact that N partitioned tasks corresponds to N processors, which implies the limitation, in which the number of load processes does not exceed a number of partitions to be loaded. Note that fig. 2 corresponds to fig. 3 in that records loaded into memory are to be part of the portion from which tasks are created (col. 5, lines 58 – 60) and subsequently, divided in to partitions for load processes, as shown in fig. 3.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to integrate the feature as taught by Bordonaro to the invention of Bhattacharya so that various memory constraints would still be suitable to apply the desired processes (Bordonaro: col. 1, lines 33 – 56).

13. **Claim 5** is rejected based on the indicated rational above since Bordonaro comprehensively taught both load (described above) and sort processes (col. 1, lines 57 – 68), which are then processed by the N processors.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to realize the advantage of combining the features disclosed by Bordonaro to the invention of Bhattacharya for overall efficiency purposes.

14. Regarding **claim 6**, Bhattacharya did not teach the memory utilized by the load and sort processes does not exceed memory constraints. Nevertheless, Bordonaro teaches the load and sort processes directly dependent on memory constraints (col. 5, lines 54 – 62).

This is considered obvious to one pertaining an ordinary skill in the art to recognize that in designing computer system to load data, in which balancing the loads become an issue, to take into account the memory constraints.

15. **Claims 23 – 25, and 42 – 44** are rejected on the same ground as stated above.

16. Claims 7 – 11, 26 – 30 and 45 - 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bhattacharya et al. (US Pat 5,797,000, hereinafter Bhattacharya) as applied to claims 1, 20, and 39 above, in view of an "Official Notice".

17. Regarding **claims 7 – 11, 26 – 30, and 45 – 49**, Bhattacharya did not teach the additional limitations as claimed. Nevertheless, the examiner takes an "Official Notice" that the limitations narrowed by these claims are considered obvious and furthermore a matter of design choice, since applicants have not disclosed that the claimed limitations solve any stated problem or are for any particular purpose and it appears that the invention would perform equally well without the claimed features. Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to efficiently utilize all the processing capabilities required for the desired task.

Allowable Subject Matter

18. **Claims 12 – 19, 31 – 38, and 50 - 57** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

19. Applicant's arguments filed 12/30/03 have been fully considered but they are not persuasive for the reasons set forth below.

20. In response to applicants' remarks, page 20, lines 1 – 3, and page 22, 4th paragraph, regarding Bayer, Tsuchida and Bhattacharya references do not teach or suggest the limitation "determining a number of load and sort processes to be started parallel based on the identified memory constraints and processing capabilities", this has already been addressed as stated in the rejection above.

Additionally, Tsuchida's fig. 2 teaches a plurality of processors implementing parallel operations in a database management system. Fig 3 teaches management node 12 determines the distribution process with the retrieval data (loading process) by execution on the basis of number of load and sort process (col. 10, line 60 – col. 11, line 16). Tsuchida also teaches of dynamic optimization process to produce an optimal result within the system processing capabilities by analyzing the processing procedures that are applicable based on the constraints (fig. 11f, 12b) including calculating the processing time considering each system characteristic (col. 3, lines 6 – 47, col. 12, lines 9 – 35).

Furthermore, applicants' arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

21. Because applicants have failed to challenge any of the Examiner's "Official Notices" in a proper and seasonably manner, they are now considered as admitted prior art. See MPEP 2144.03.

Conclusion

22. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lilian Vo whose telephone number is 703-305-7864. The examiner can normally be reached on Monday - Thursday, 7:30am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on 703-305-9678. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lilian Vo
Examiner
Art Unit 2127

lv
March 2, 2004

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